OIPE JC105 JUL 19 2004 PATENT & TRADEMARK OFFICE

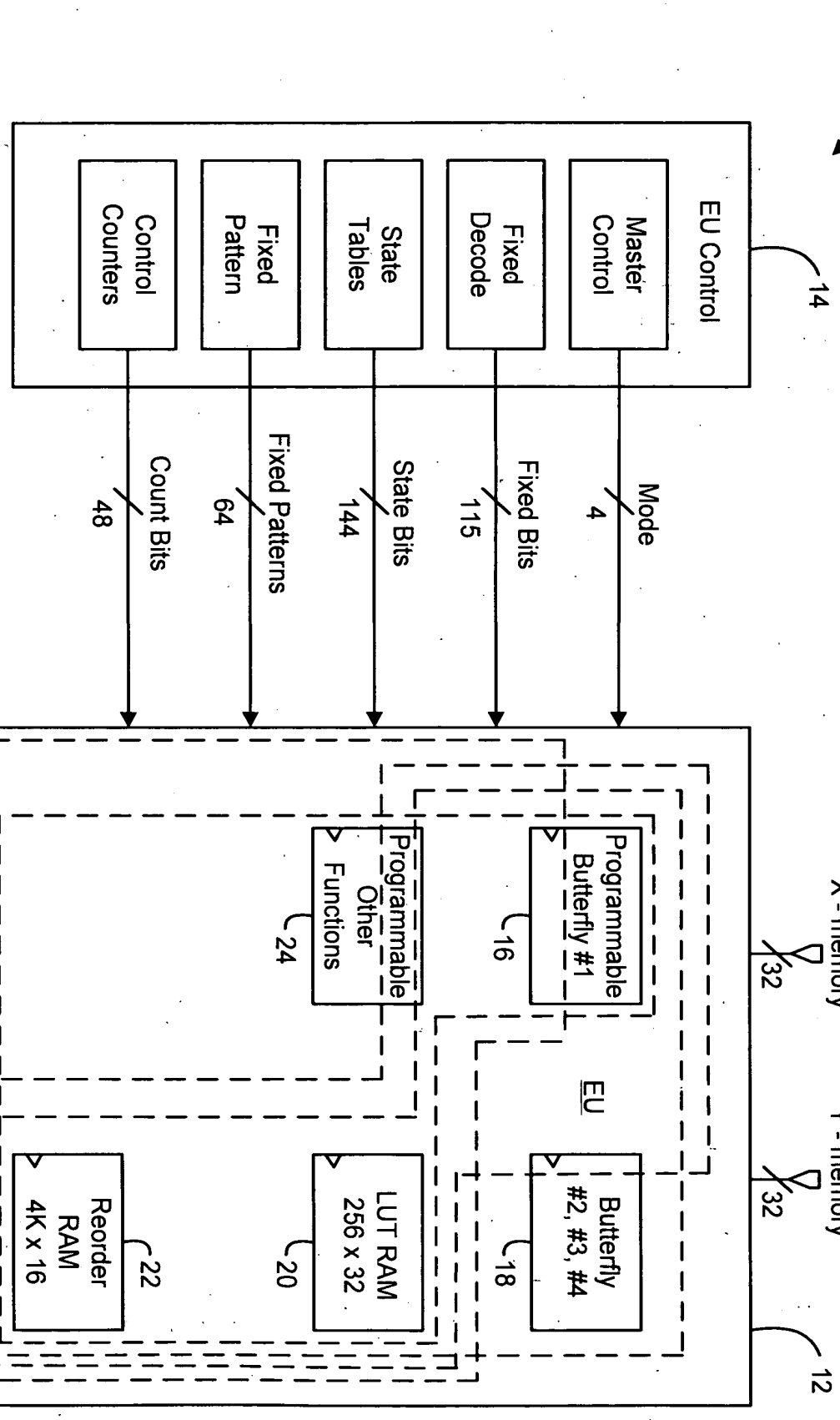



Fig. 1a

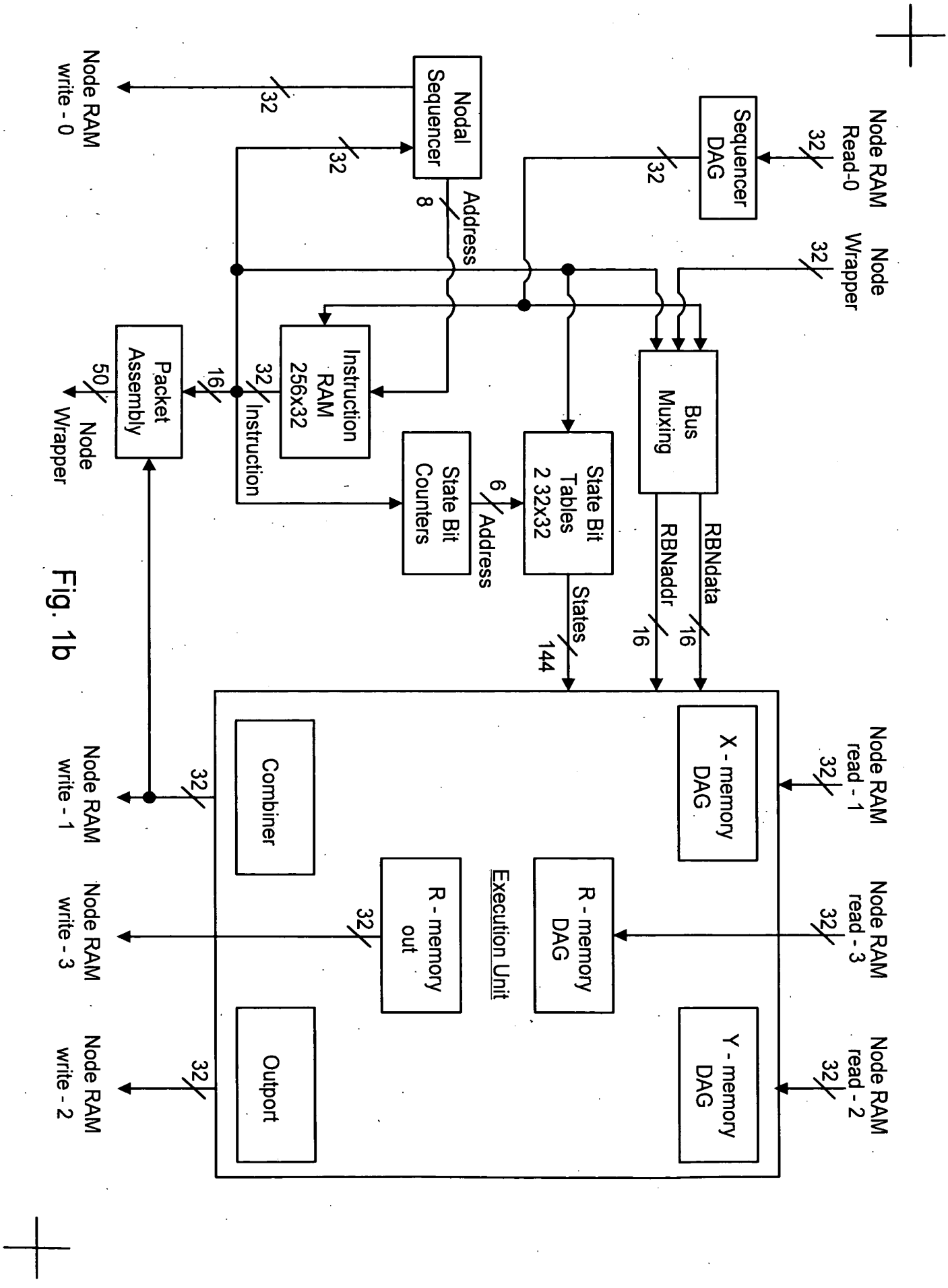

Node RAM Read-0
32
Sequencer DAG
32
Node Wrapper
32
Node RAM write - 0
32
Nodal Sequencer
32
8
Address
Bus Muxing
RBNdata
16
RBNaddr
16
States
144
State Bit Tables 2 32x32
6
Address
State Bit Counters
Instruction RAM 256x32
32
Instruction
16
Packet Assembly
50
Node Wrapper
Node RAM read - 1
32
X - memory DAG
Node RAM read - 3
32
R - memory DAG
Node RAM read - 2
32
Y - memory DAG
Execution Unit
Combiner
32
Node RAM write - 1
R - memory out
32
Node RAM write - 3
Outport
32
Node RAM write - 2

Fig. 1b

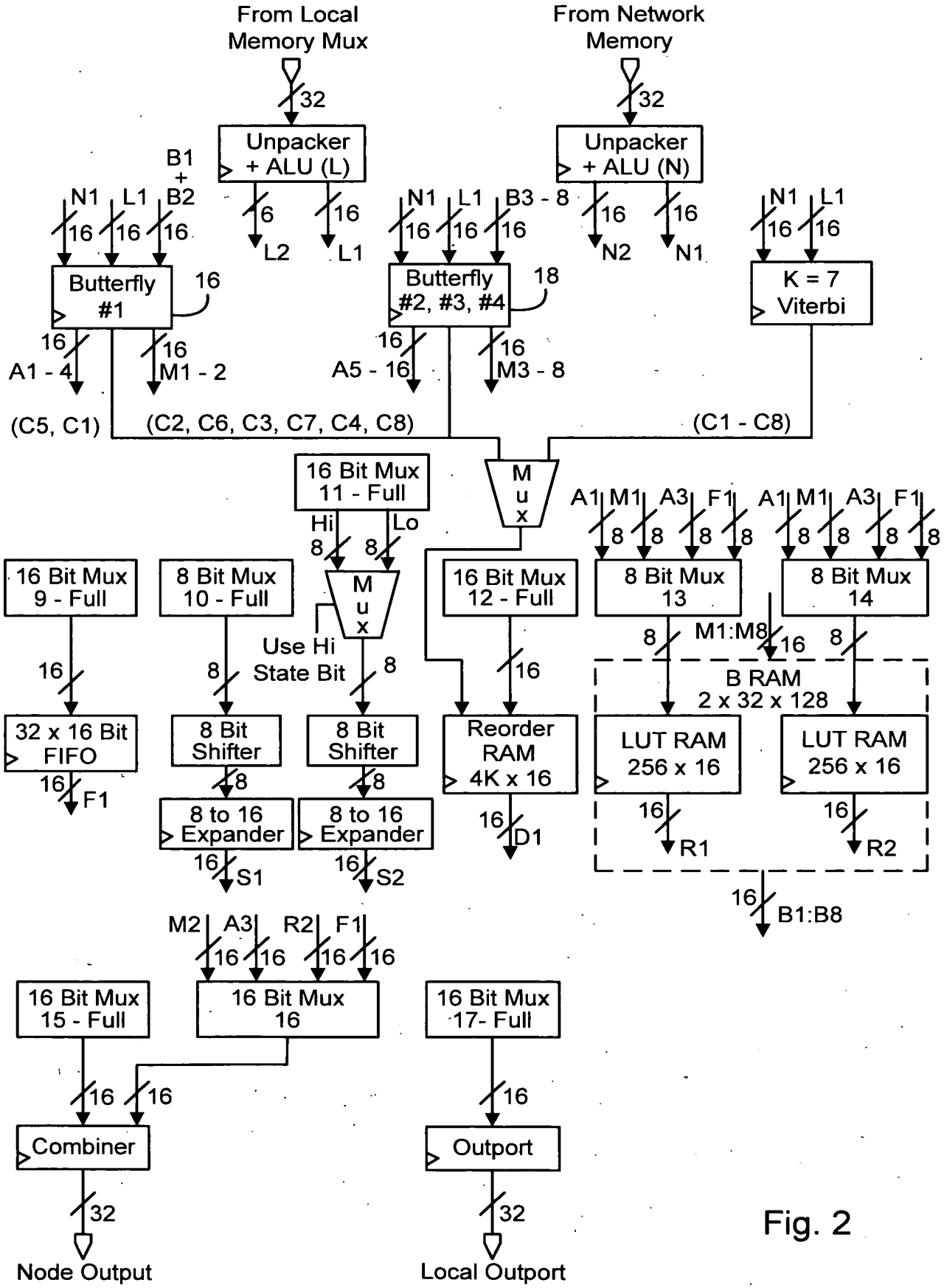

From Local Memory Mux
From Network Memory
32
32
Unpacker + ALU (L)
Unpacker + ALU (N)
B1 + B2
N1 L1
B3 - 8
N1 L1
N1 L1
16 16 16
16 16 16
16 16
16 16
16 16
6
16
L2
L1
N2
N1
Butterfly #1
16
Butterfly #2, #3, #4
18
K = 7 Viterbi
16
16
16
16
16
16
A1 - 4
M1 - 2
A5 - 16
M3 - 8
(C5, C1)
(C2, C6, C3, C7, C4, C8)
(C1 - C8)
16 Bit Mux 11 - Full
Hi
Lo
8
8
M u x
A1 M1 A3 F1
A1 M1 A3 F1
8 8 8 8
8 8 8 8
16 Bit Mux 9 - Full
8 Bit Mux 10 - Full
M u x
16 Bit Mux 12 - Full
8 Bit Mux 13
8 Bit Mux 14
Use Hi State Bit
8
M1:M8
16
8
16
8
8
16
B RAM 2 x 32 x 128
32 x 16 Bit FIFO
8 Bit Shifter
8 Bit Shifter
Reorder RAM 4K x 16
LUT RAM 256 x 16
LUT RAM 256 x 16
16
F1
8
8
16
16
16
16
R1
R2
8 to 16 Expander
8 to 16 Expander
D1
16
S1
16
S2
16
B1:B8
M2 A3 R2 F1
16 16 16 16
16 Bit Mux 15 - Full
16 Bit Mux 16
16 Bit Mux 17- Full
16 16
16
Combiner
Outport
32
32
Node Output
Local Outport

Fig. 2

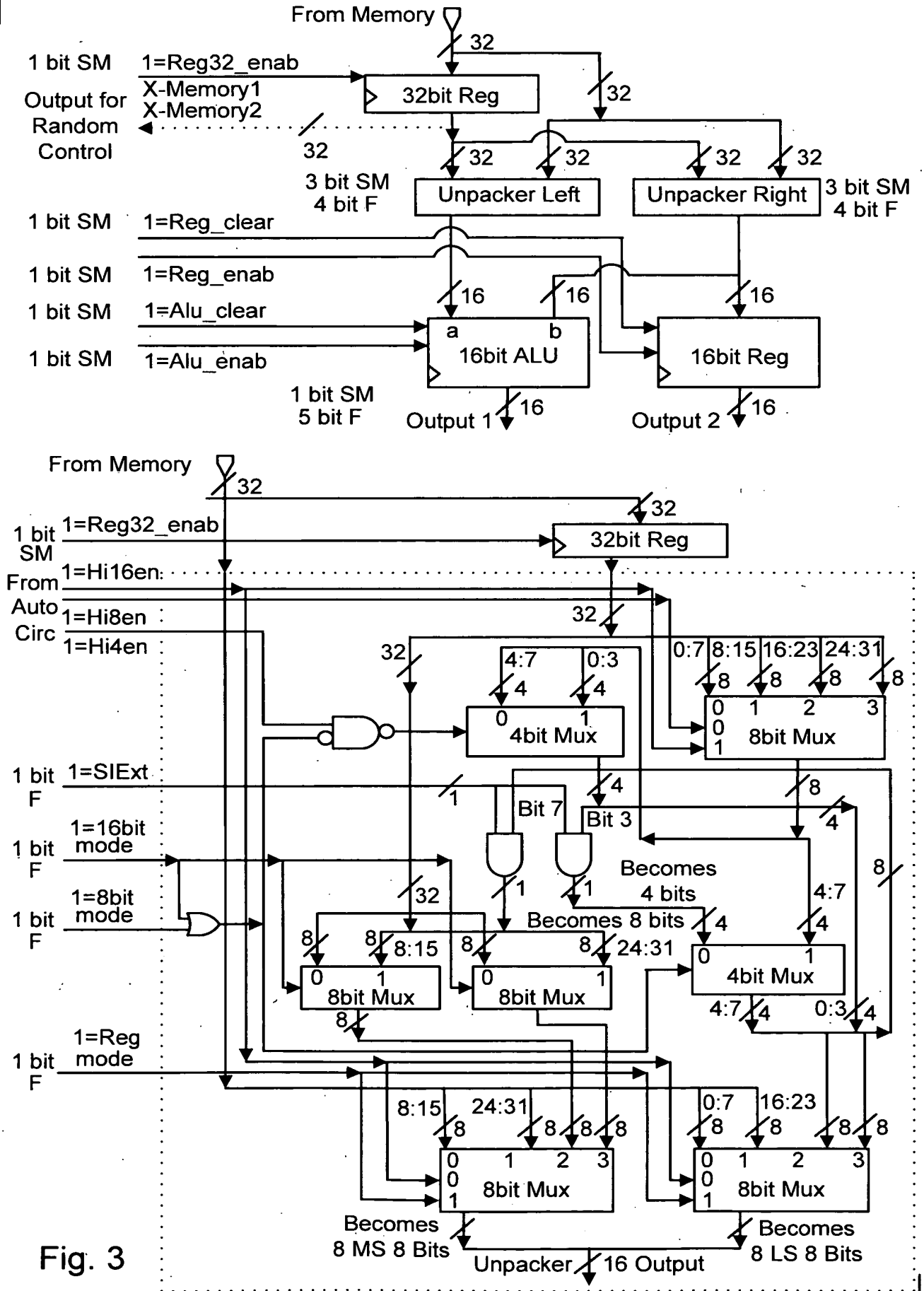

From Memory
32
1 bit SM
1=Reg32_enab
32bit Reg
Output for Random Control
X-Memory1
X-Memory2
32
3 bit SM
4 bit F
Unpacker Left
Unpacker Right
1 bit SM
1=Reg_clear
1 bit SM
1=Reg_enab
1 bit SM
1=Alu_clear
1 bit SM
1=Alu_enab
16
a
b
16bit ALU
16bit Reg
1 bit SM
5 bit F
Output 1
Output 2
From Memory
1 bit SM
1=Reg32_enab
From Auto Circ
1=Hi16en
1=Hi8en
1=Hi4en
1 bit F
1=SIExt
1=16bit mode
1=8bit mode
1=Reg mode
4:7
0:3
4bit Mux
8bit Mux
0:7
8:15
16:23
24:31
Bit 7
Bit 3
Becomes 4 bits
Becomes 8 bits
Becomes 8 MS 8 Bits
Becomes 8 LS 8 Bits
Unpacker 16 Output

Fig. 3

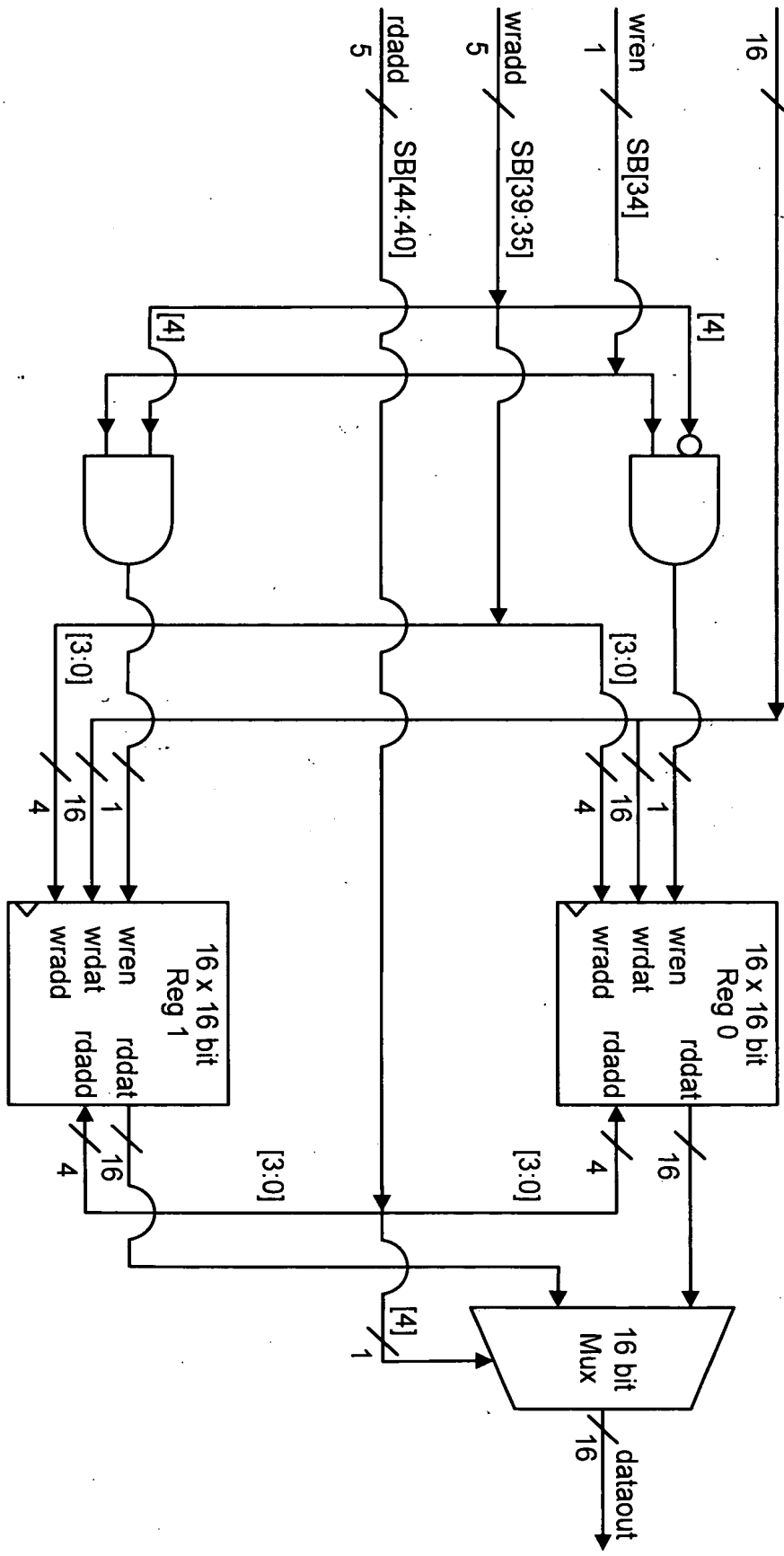

Mux Datain
16
wren
1
SB[34]
wradd
5
SB[39:35]
rdadd
5
SB[44:40]
[4]
[4]
[3:0]
[3:0]
4
16
1
4
16
1
16 x 16 bit Reg 0
wren
wrdat
wradd
rdadd
rddat
16 x 16 bit Reg 1
wren
wrdat
wradd
rdadd
rddat
[3:0]
[3:0]
4
16
4
16
[4]
1
16 bit Mux
16
dataout

Fig. 4

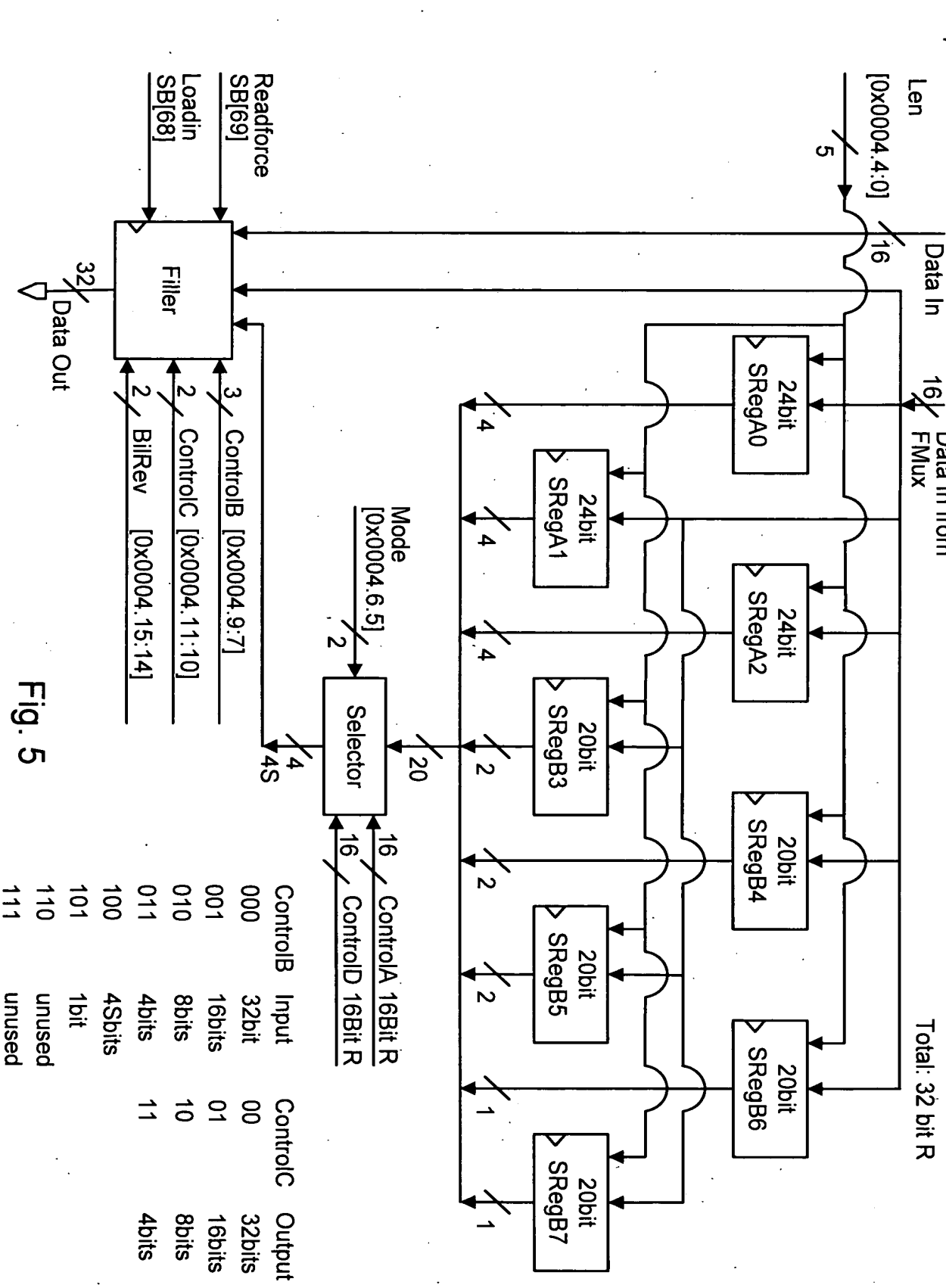



Fig. 5

| ControlB | Input | ControlC | Output |
|---|---|---|---|
| 000 | 32bit | 00 | 32bits |
| 001 | 16bits | 01 | 16bits |
| 010 | 8bits | 10 | 8bits |
| 011 | 4bits | 11 | 4bits |
| 100 | 4Sbits | | |
| 101 | 1bit | | |
| 110 | unused | | |
| 111 | unused | | |

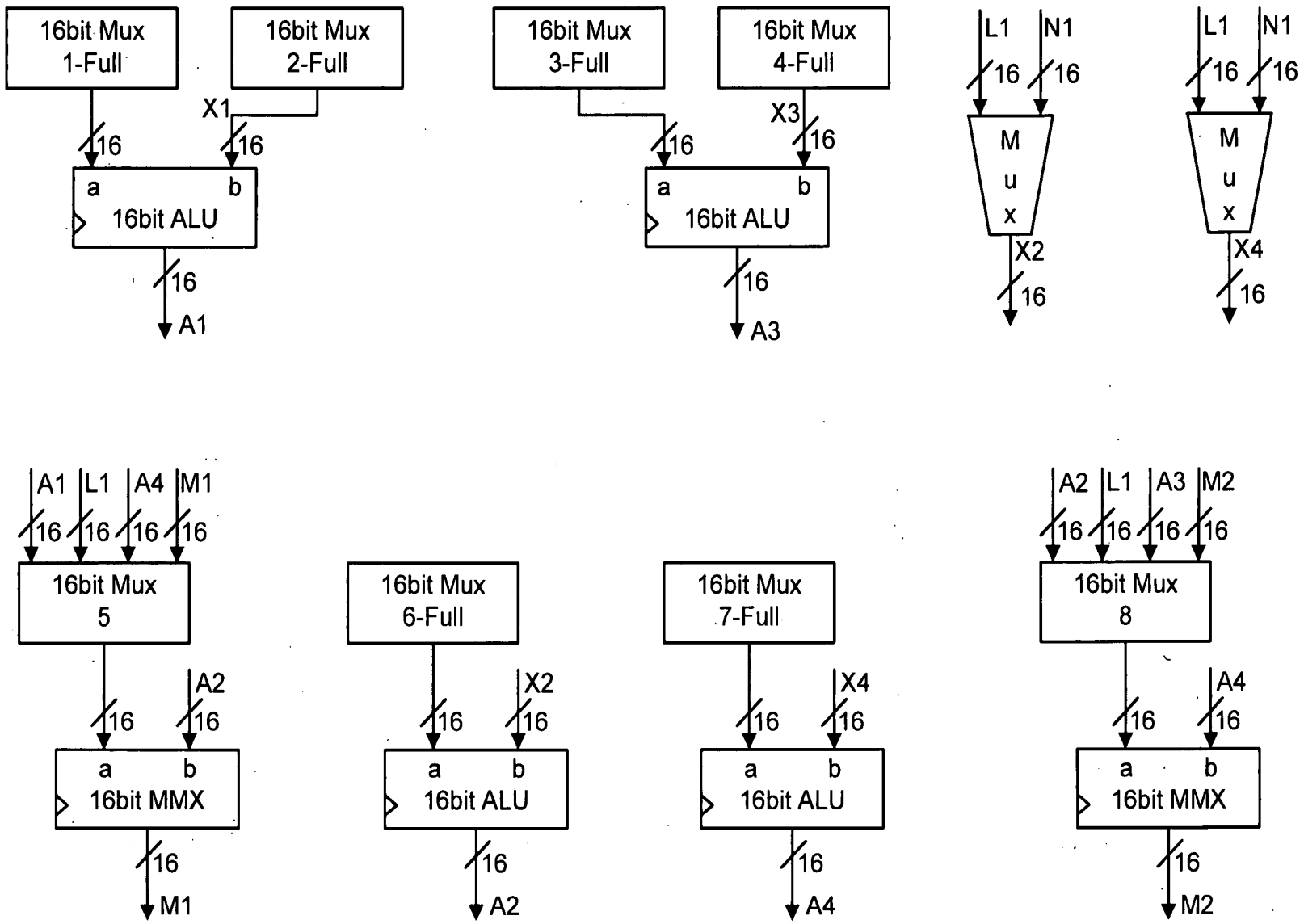

16bit Mux
1-Full
16bit Mux
2-Full
X1
16
16
a
b
16bit ALU
16
A1
16bit Mux
3-Full
16bit Mux
4-Full
X3
16
16
a
b
16bit ALU
16
A3
L1
N1
16
16
M
u
x
X2
16
L1
N1
16
16
M
u
x
X4
16
A1
L1
A4
M1
16
16
16
16
16bit Mux
5
A2
16
16
a
b
16bit MMX
16
M1
16bit Mux
6-Full
X2
16
16
a
b
16bit ALU
16
A2
16bit Mux
7-Full
X4
16
16
a
b
16bit ALU
16
A4
A2
L1
A3
M2
16
16
16
16
16bit Mux
8
A4
16
16
a
b
16bit MMX
16
M2

Fig. 6a

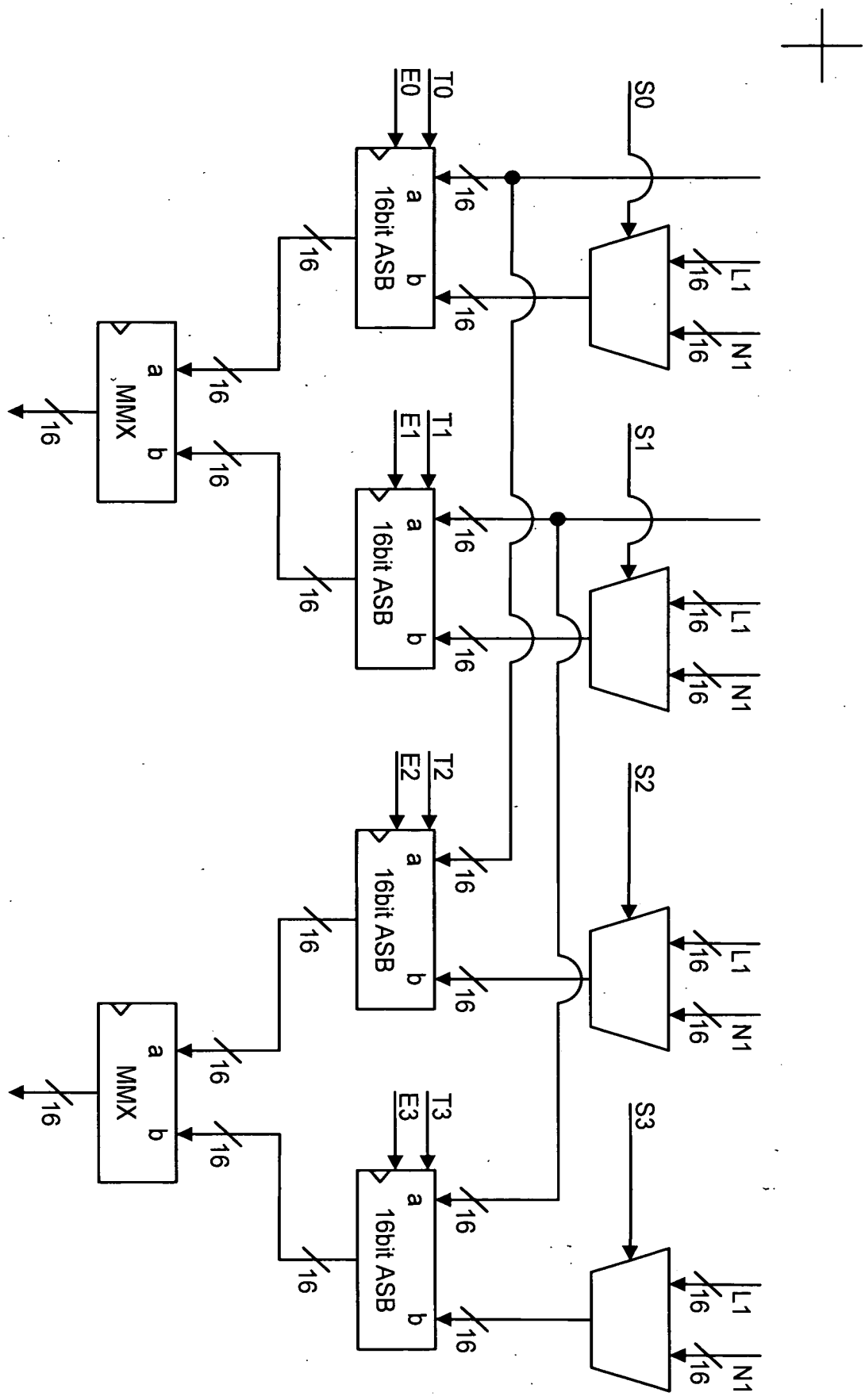



Fig. 6b

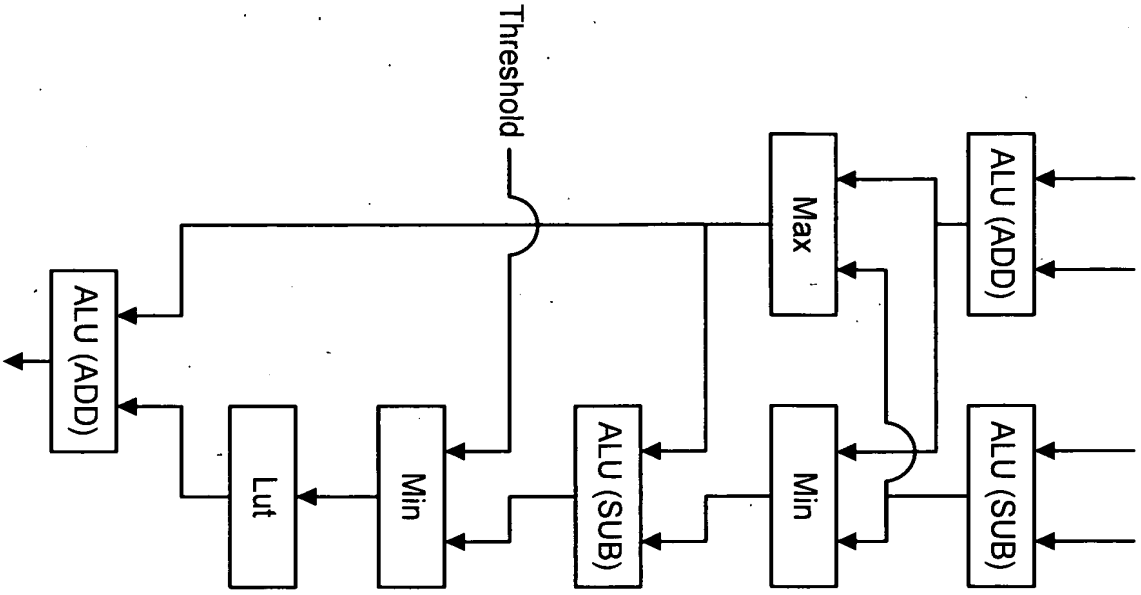

ALU (ADD)
ALU (SUB)
Max
Min
Threshold
ALU (SUB)
Min
Lut
ALU (ADD)

Fig. 7a

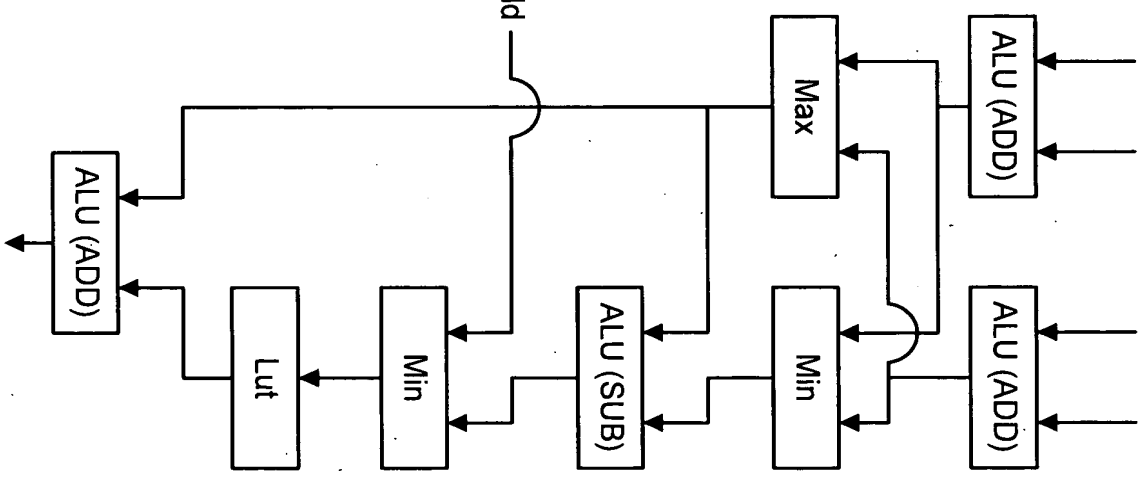

ALU (ADD)
ALU (ADD)
Max
Min
Threshold
ALU (SUB)
Min
Lut
ALU (ADD)

Fig. 7b

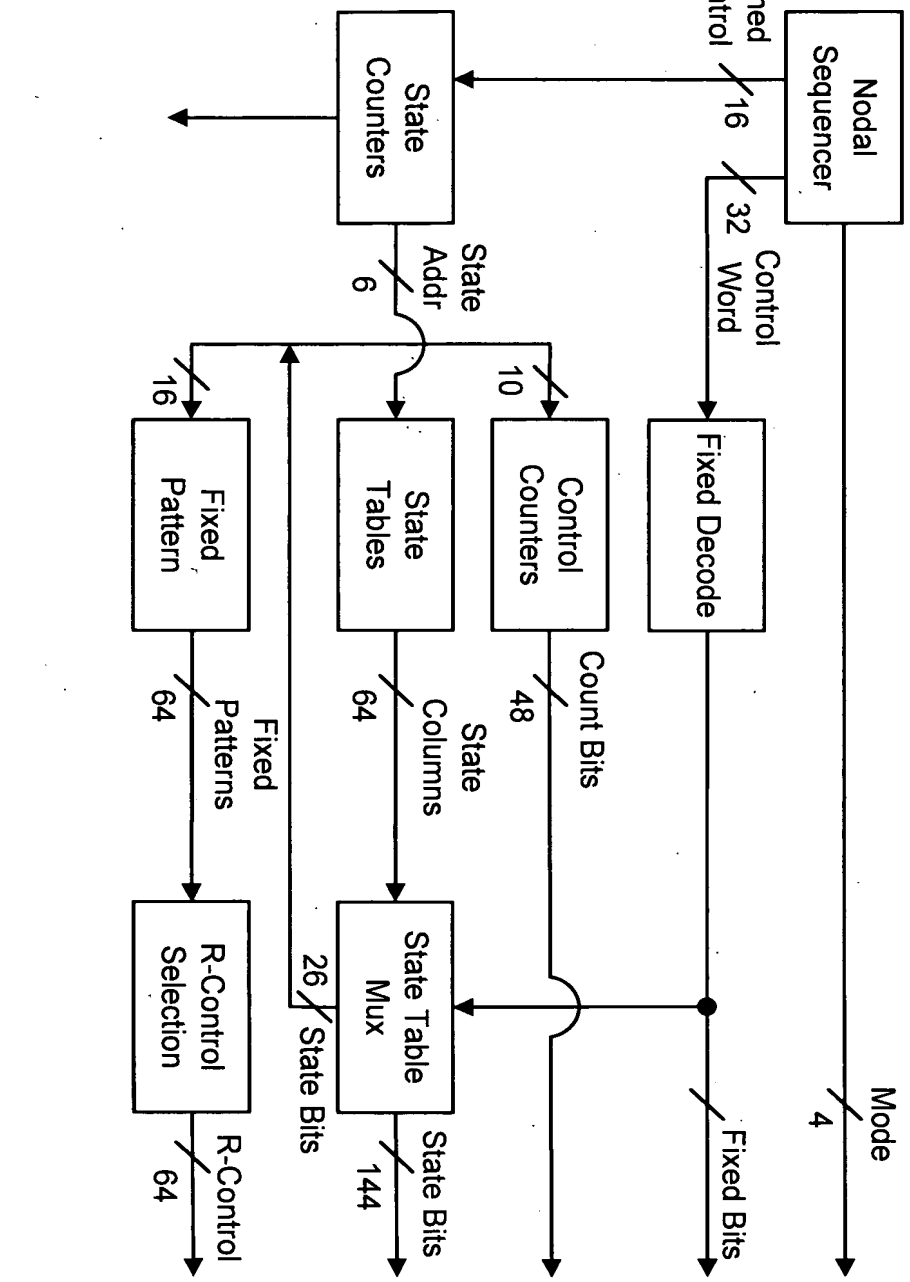

Nodal Sequencer
Immed Control
16
32
Control Word
Mode
4
State Counters
State Addr
6
10
16
Fixed Decode
Control Counters
State Tables
Fixed Pattern
Fixed Bits
Count Bits
48
State Columns
64
Fixed Patterns
64
State Table Mux
26
State Bits
State Bits
144
R-Control Selection
R-Control
64

Fig. 8a

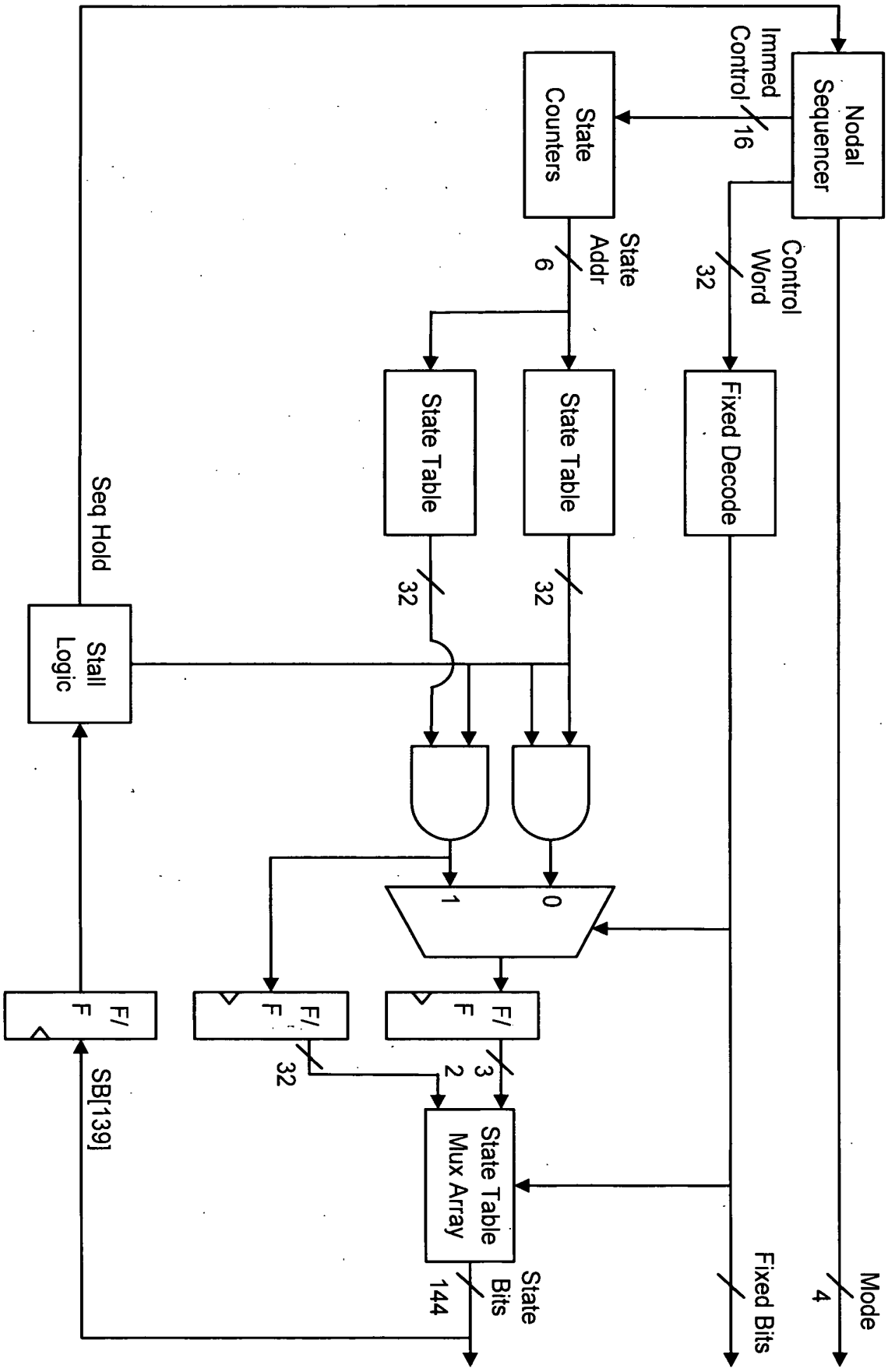

Nodal Sequencer
Immed Control
16
State Counters
State Addr
6
Control Word
32
Fixed Decode
State Table
State Table
32
32
Seq Hold
Stall Logic
1
0
F/F
F/F
F/F
32
3
2
State Table Mux Array
State Bits
144
Fixed Bits
Mode
4
SB[139]

Fig. 8b

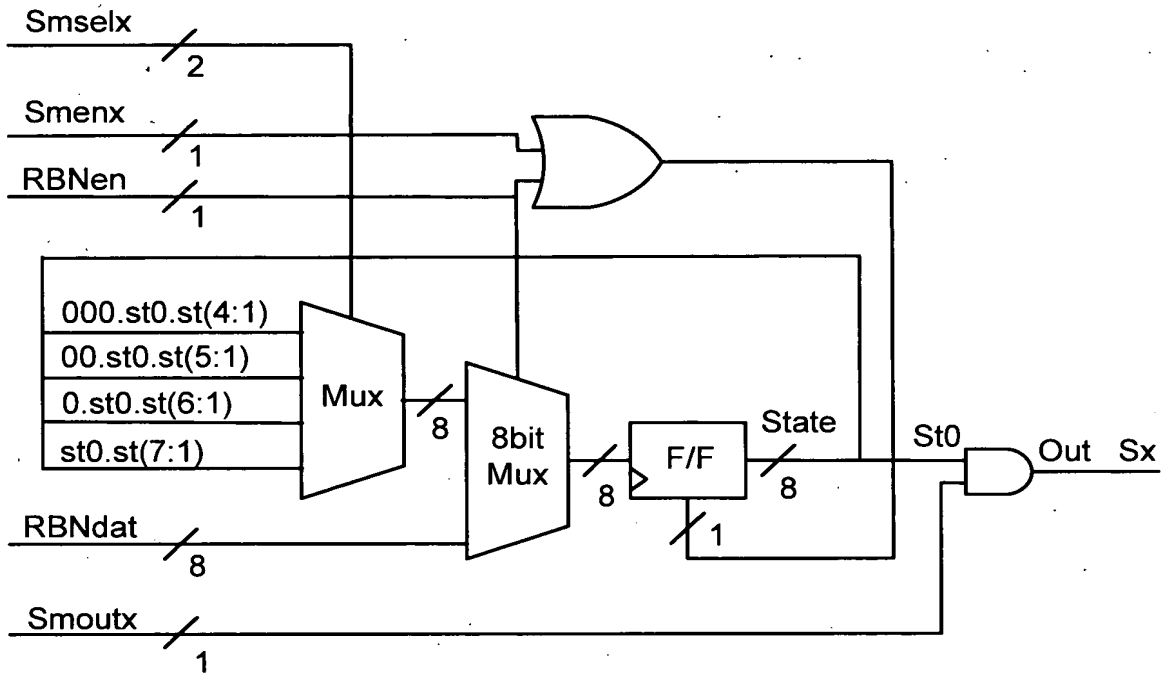

Smselx
2
Smenx
1
RBNen
1
000.st0.st(4:1)
00.st0.st(5:1)
0.st0.st(6:1)
st0.st(7:1)
Mux
8
8bit
Mux
8
F/F
State
8
St0
Out
Sx
1
RBNdat
8
Smoutx
1

Fig. 9

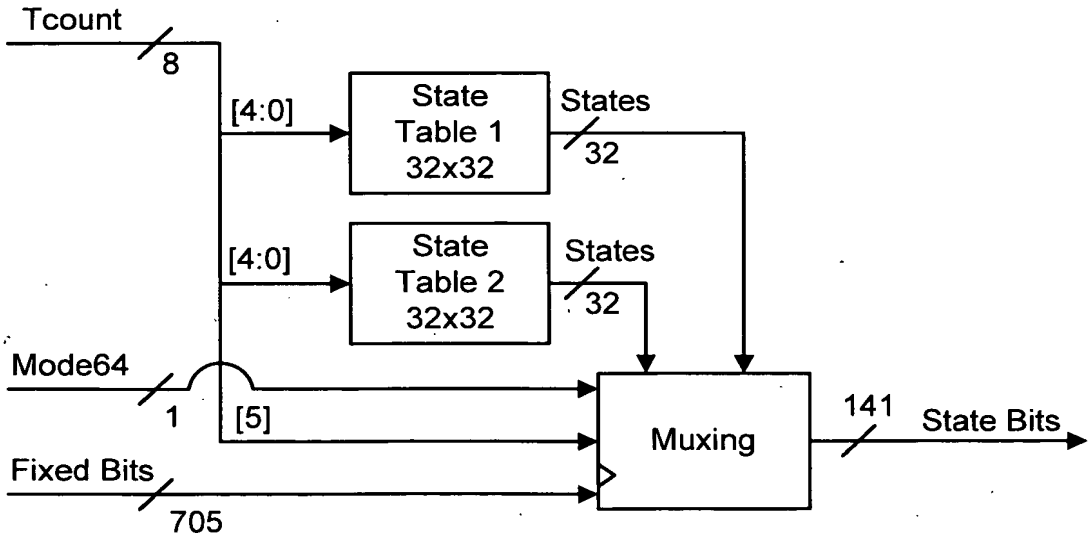
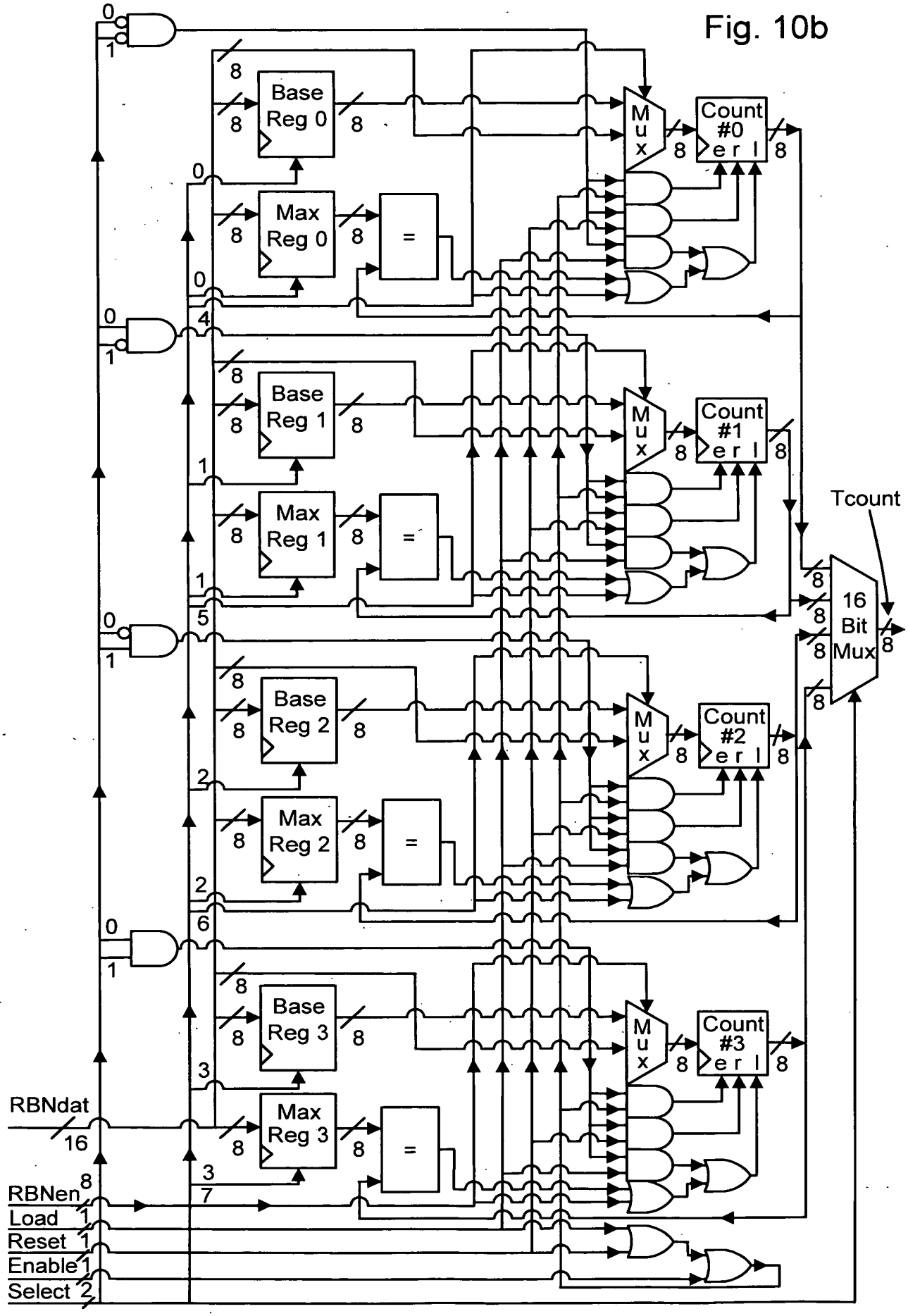

Tcount
8
[4:0]
State
Table 1
32x32
States
32
[4:0]
State
Table 2
32x32
States
32
Mode64
1
[5]
Fixed Bits
705
Muxing
141
State Bits

Fig. 10a

Fig. 10b


Base Reg 0
Max Reg 0
Count #0
Base Reg 1
Max Reg 1
Count #1
Base Reg 2
Max Reg 2
Count #2
Base Reg 3
Max Reg 3
Count #3
Mux
=
Tcount
16 Bit Mux
RBNdat
16
RBNen
Load
Reset
Enable
Select
8
1
2

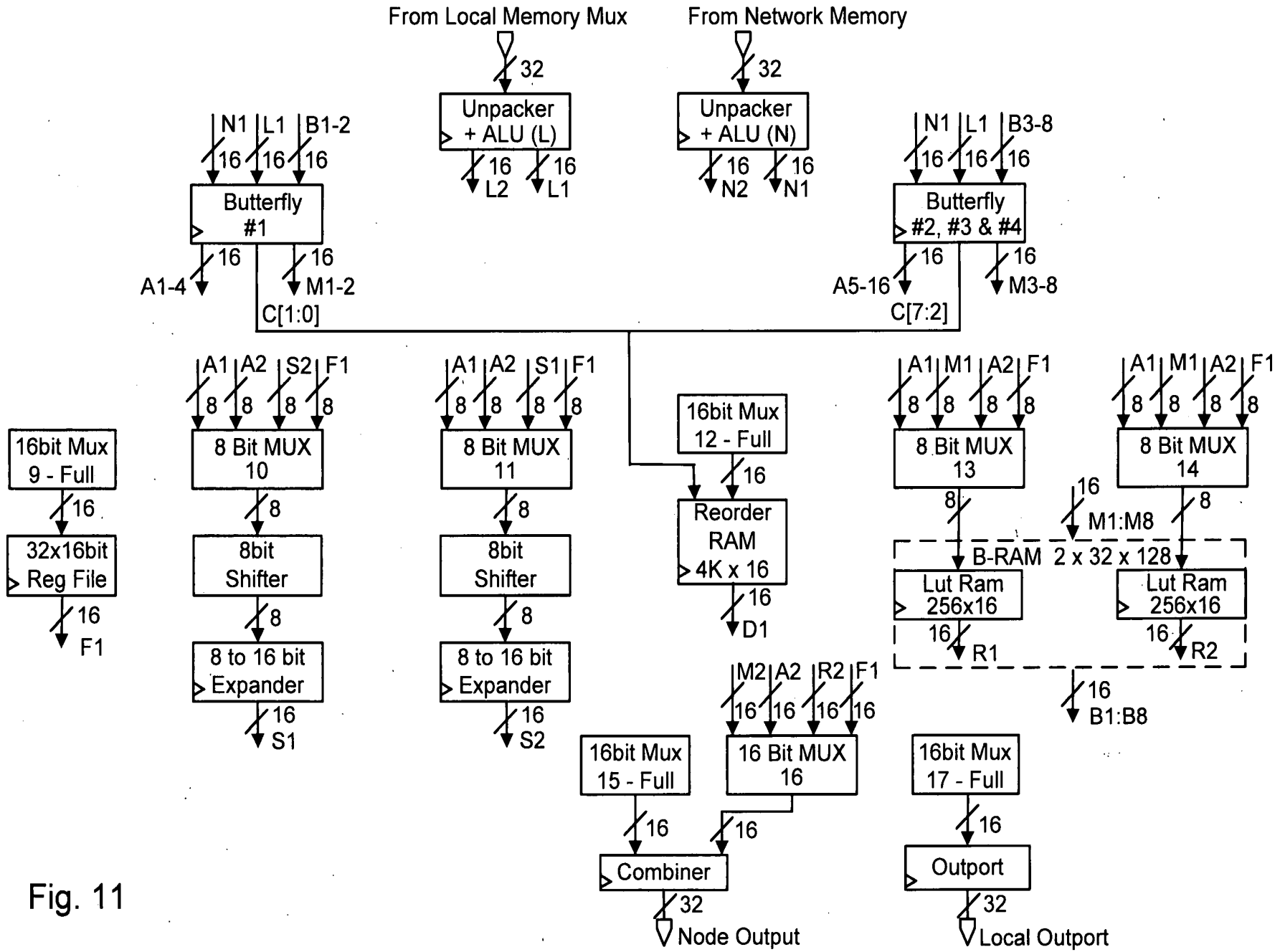

From Local Memory Mux
From Network Memory
32
Unpacker + ALU (L)
Unpacker + ALU (N)
16 L2
16 L1
16 N2
16 N1
N1 L1 B1-2
Butterfly #1
A1-4
M1-2
C[1:0]
N1 L1 B3-8
Butterfly #2, #3 & #4
A5-16
M3-8
C[7:2]
16bit Mux 9 - Full
32x16bit Reg File
F1
A1 A2 S2 F1
8 Bit MUX 10
8bit Shifter
8 to 16 bit Expander
S1
A1 A2 S1 F1
8 Bit MUX 11
8bit Shifter
8 to 16 bit Expander
S2
16bit Mux 12 - Full
Reorder RAM 4K x 16
D1
A1 M1 A2 F1
8 Bit MUX 13
A1 M1 A2 F1
8 Bit MUX 14
M1:M8
B-RAM 2 x 32 x 128
Lut Ram 256x16
R1
Lut Ram 256x16
R2
B1:B8
M2 A2 R2 F1
16 Bit MUX 16
16bit Mux 15 - Full
Combiner
Node Output
16bit Mux 17 - Full
Outport
Local Outport

Fig. 11

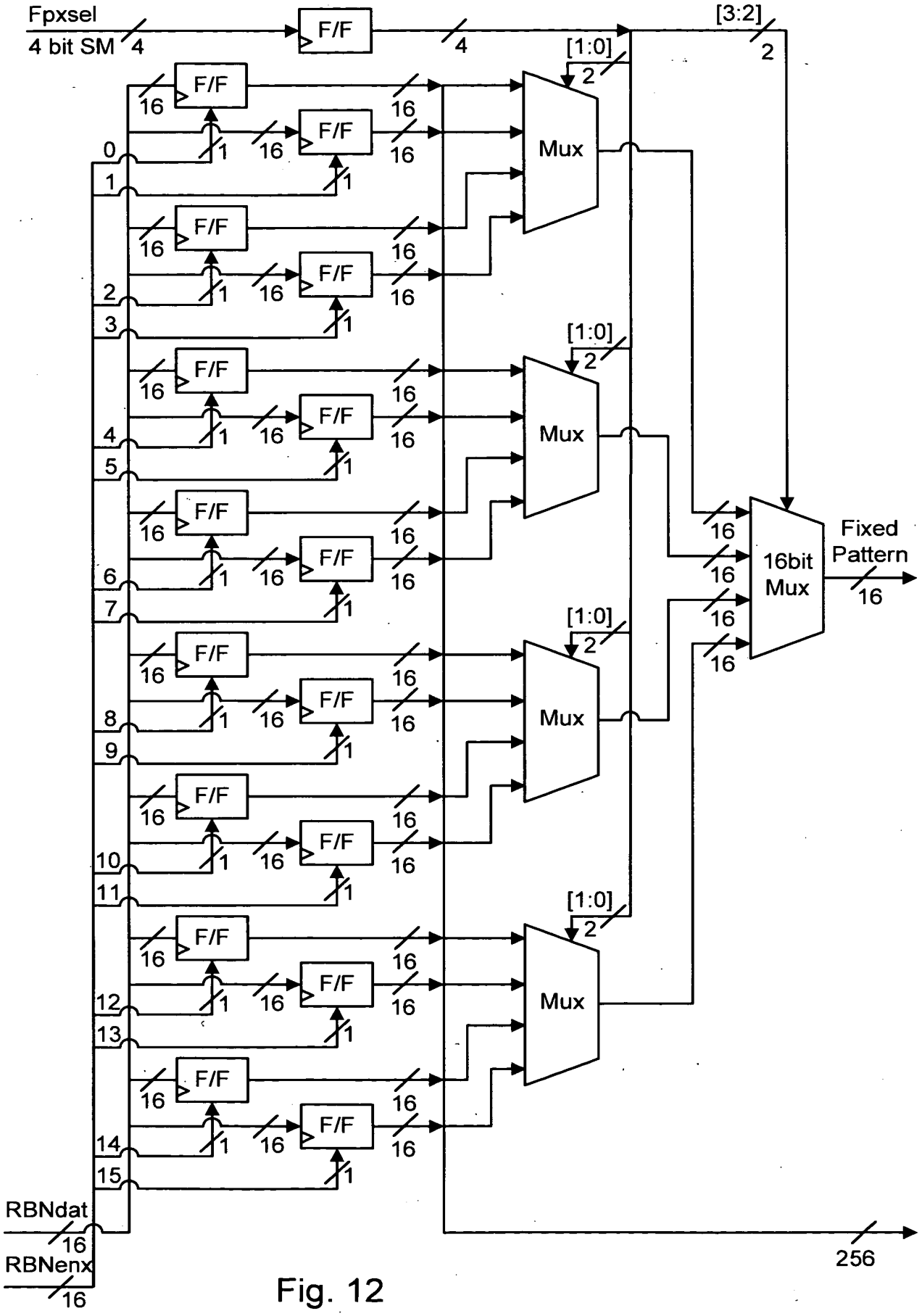

Fpxsel
4 bit SM
4
F/F
4
[3:2]
2
[1:0]
2
Mux
16bit Mux
Fixed Pattern
16
F/F
16
1
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
RBNdat
16
RBNenx
16
256

Fig. 12

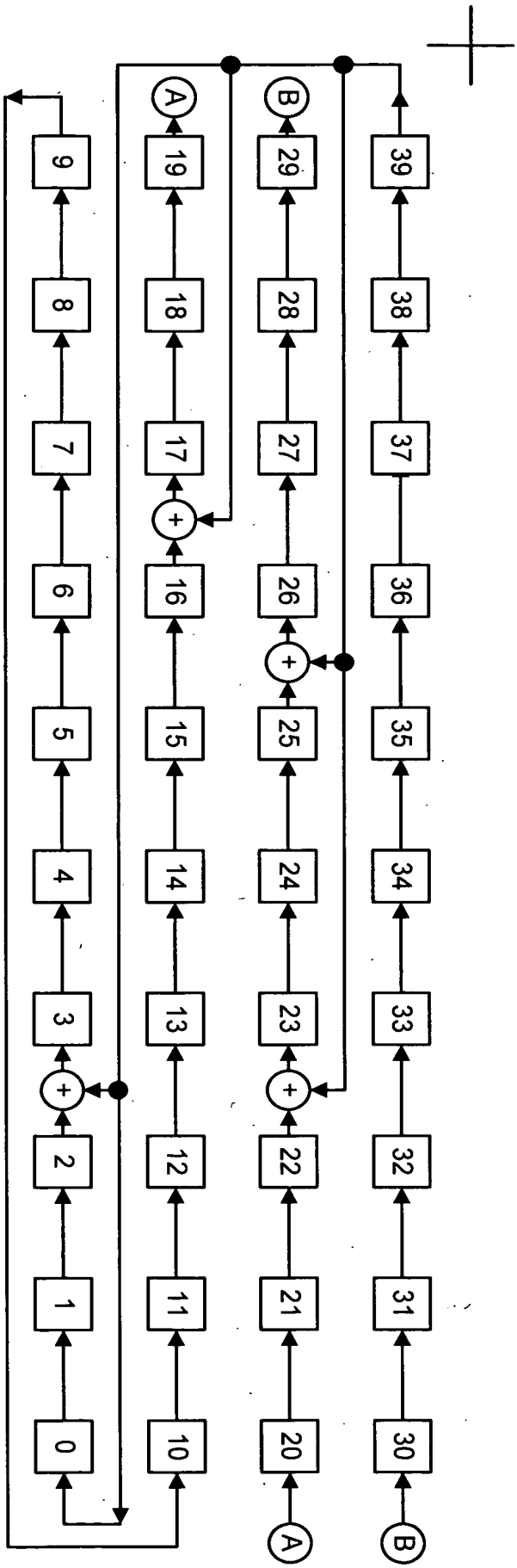

39
38
37
36
35
34
33
32
31
30
B
29
28
27
26
25
24
23
22
21
20
A
19
18
17
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
+

Fig. 13

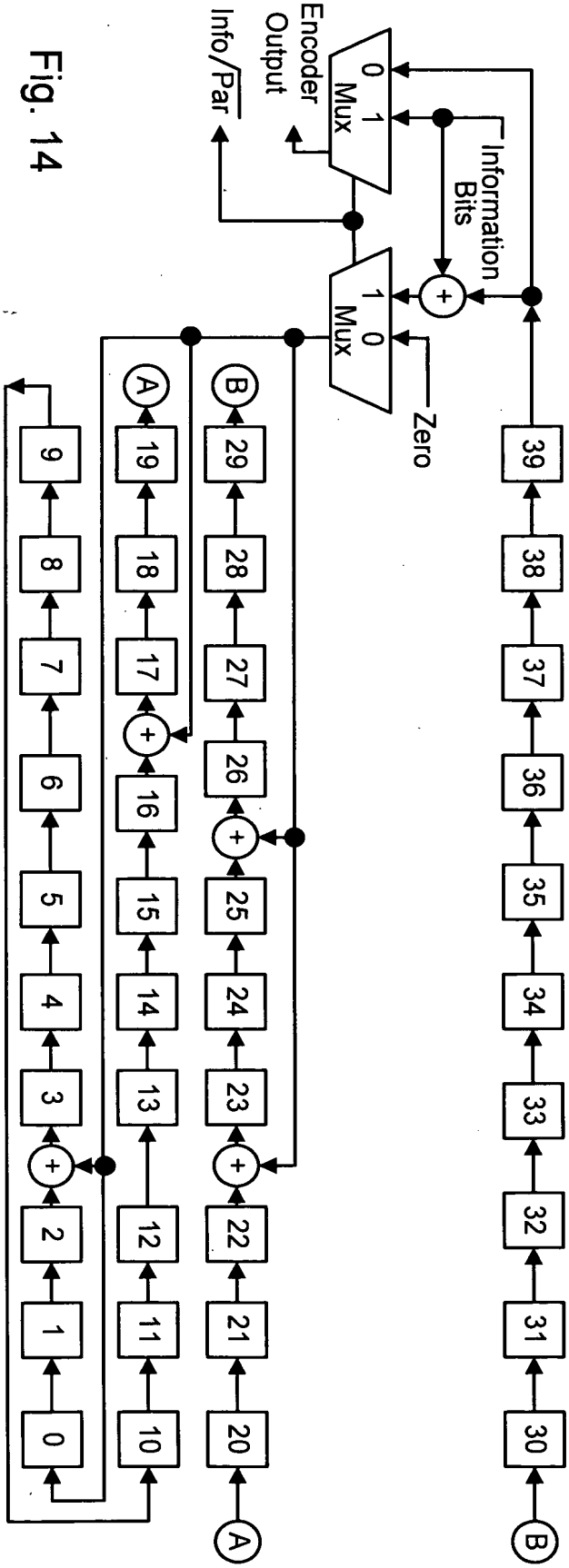

Encoder Output
Info/Par
Mux
0 1
1 0
Information Bits
Zero
+
39
38
37
36
35
34
33
32
31
30
B
29
28
27
26
25
24
23
22
21
20
A
19
18
17
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0

Fig. 14

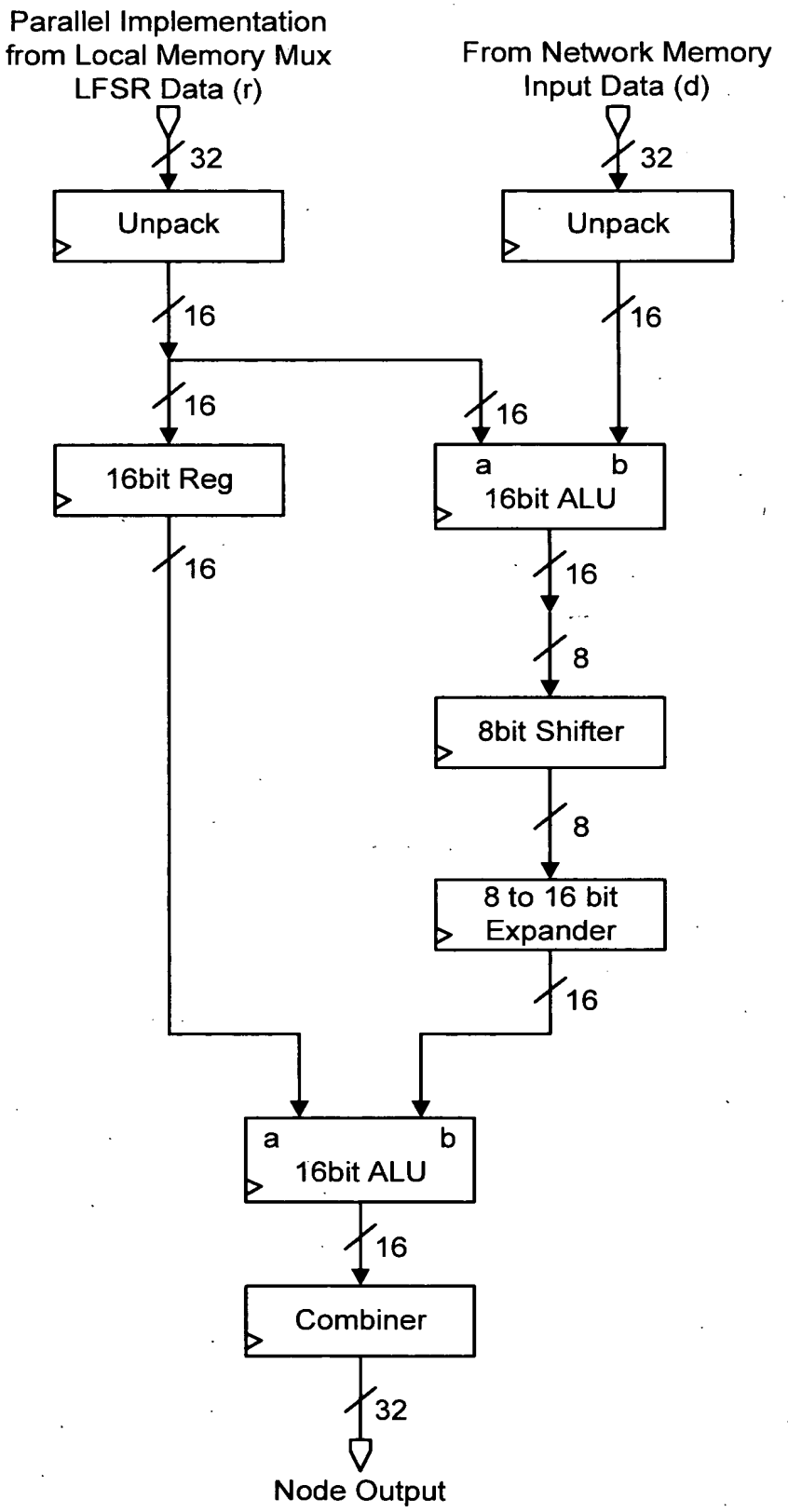

Parallel Implementation
from Local Memory Mux
LFSR Data (r)
From Network Memory
Input Data (d)
32
32
Unpack
Unpack
16
16
16
16
16bit Reg
a
b
16bit ALU
16
16
8
8bit Shifter
8
8 to 16 bit
Expander
16
a
b
16bit ALU
16
Combiner
32
Node Output

Fig. 15

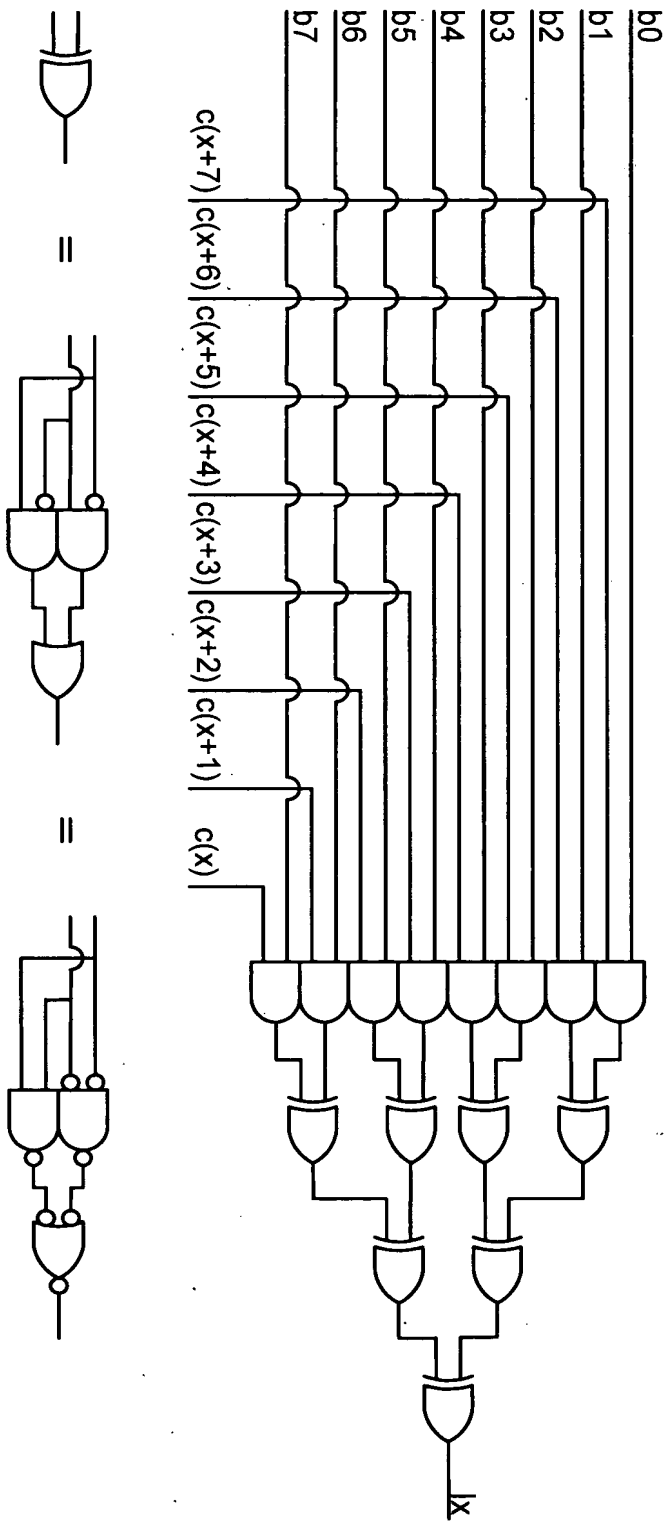



Fig. 16

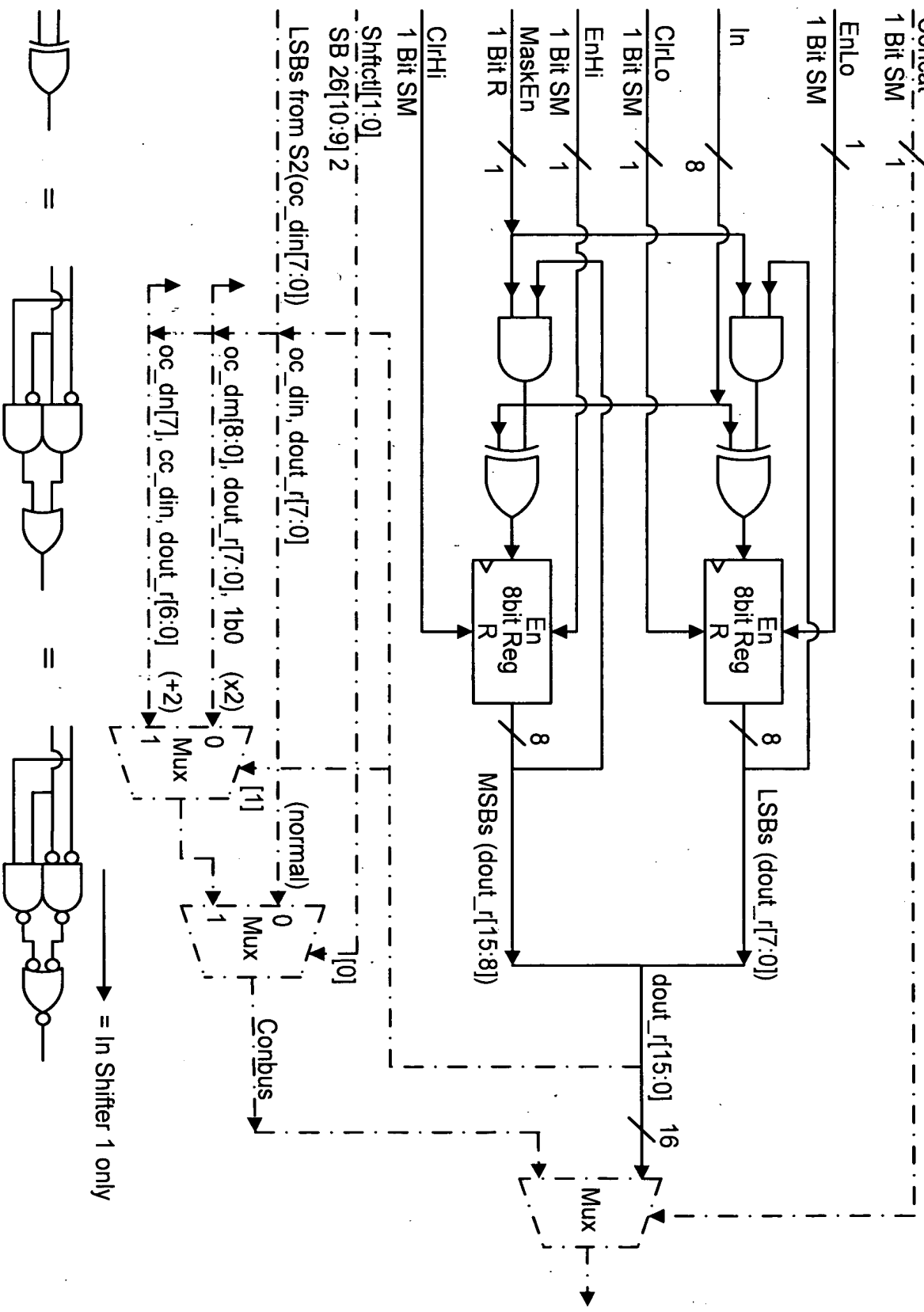

Concat
1 Bit SM
EnLo
1 Bit SM
In
8
ClrLo
1 Bit SM
EnHi
1 Bit SM
MaskEn
1 Bit R
ClrHi
1 Bit SM
Shftctl[1:0]
SB 26[10:9] 2
LSBs from S2(oc_din[7:0])
oc_dm[8:0], dout_r[7:0], 1b0
oc_dn[7], cc_din, dout_r[6:0]
(x2)
(+2)
Mux
[1]
oc_din, dout_r[7:0]
(normal)
Mux
[0]
Conbus
En
8bit Reg
R
8
LSBs (dout_r[7:0])
MSBs (dout_r[15:8])
dout_r[15:0] 16
Mux
= In Shifter 1 only

Fig. 17

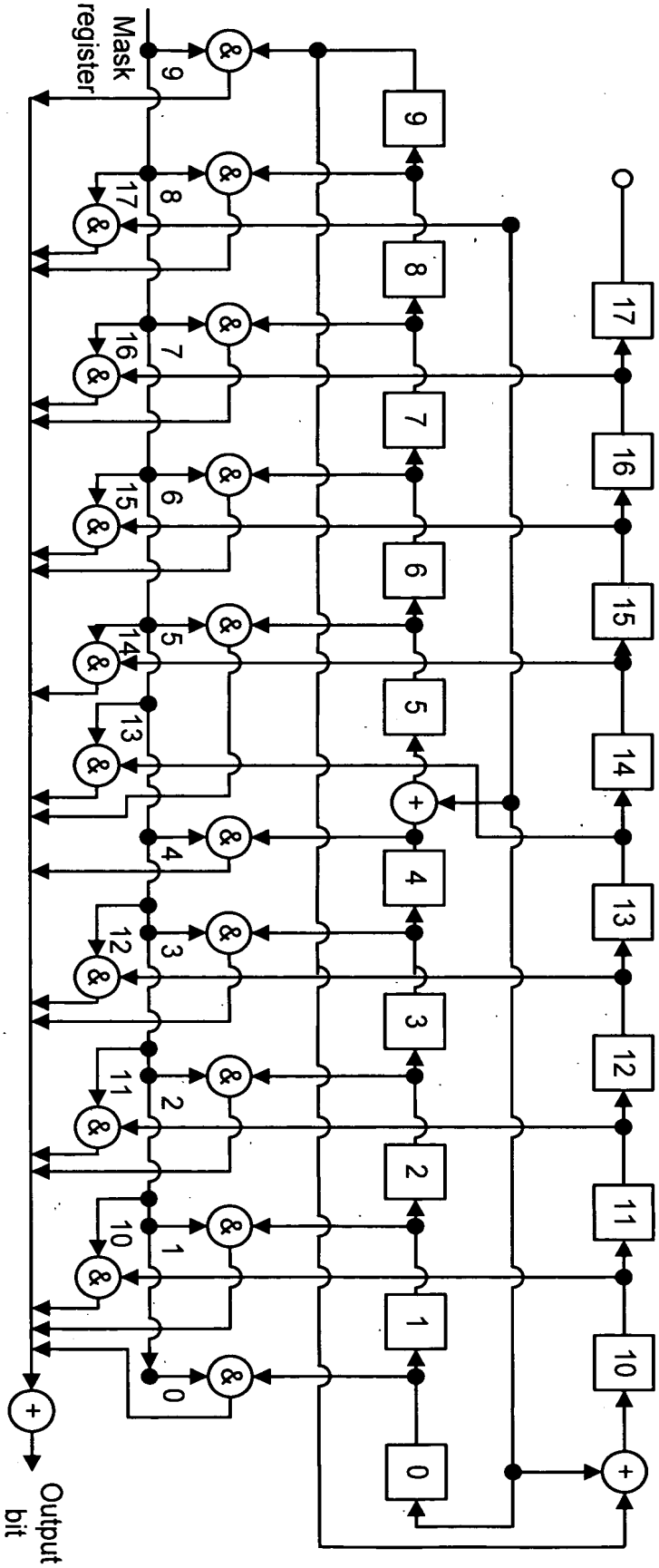



Fig. 18